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sequential

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output-z **Book Review | Digital Logic and computer Design by Morris Mano | Digital Electronics book Review**  
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and one  
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**in Fig. P5.8**  
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**Combinational**  
**Logic - Part 03**  
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**Procedure Q.**  
**5.4: A PN flip-**  
**flop has four**  
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**clear to 0, no**  
**change,**  
**complement,**  
**and set to 1,**  
**when DIGITAL**  
**SYSTEM**  
**DESIGN**  
**OVERVIEW Q.**  
**6.10: Design a**  
**serial 2's**

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*with a shift*  
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Procedure:  
Task 1: Our  
first task was

to create a  
logic diagram  
of a 4-bit  
binary adder,  
which  
consisted of  
just one chip  
titled  
"7483N",  
along with  
creating a  
truth table. I  
connected the  
A1-A4 to  
either the  
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