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ADD AX, imm16 \$05 ADD r/m8, imm8 \$80 xx000xxx (ModR/M byte) ...ECS 50 8086 Instruction Set Opcodes8086 OPCODE SHEET PDF - This is an HTML-ized version of the opcode map for the processor. It is based on the opcode map from Appendix A of Volume 2 of the Intel Architecture. 128086 OPCODE SHEET PDFOpcode Sheet for 8. Microprocessor With Description. For fans of The Hunger Games, Battlestar Galactica, and Blade Runner comes th.. See details of opcode

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Opcode Bytes 1. ACI Data
 CE 2 2. ADC A 8F 1 3. ADC
 B 88 1 4. ADC C 89 1 5.
 ADC D 8A 1 6. ADC E 8B 1
 7. ADC H 8C 1 8. ADC L
 8D 1 9. ADC M 8E 1 10.
 ADD A 87 1 11. ADD B 80
 1 12. ADD C 81 1 13.
 ...OPCODES TABLE OF
 INTEL 8085 Opcodes of
 Intel 8085 in ...8086
 Instruction Encoding-8
 Addressing Mode 00!
 Specifies R/M Table 1
 (with NO displacement)
 000 [BX+SI] 010 [BP+SP]
 100 [SI] 110 Drc't Add
 001 [BX+DI] 011 [BP+DI]
 101 [DI] 111 [BX]! Note
 that the 110 case (direct

addressing) requires that
 the instruction be
 followed by two address
 bytes There are then two
 possibilities: 1 Opcode
 Addressing ModeEncoding
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 see ADD ADD opcode +
 \$10, and xx010xxx
 (ModR/M byte) for \$80-
 \$83 ADD r/m8, reg8 \$00
 ADD r/m16, reg16 \$01
 ADD reg8, r/m8 \$02 ADD
 reg16, r/m16 \$03 ADD AL,
 imm8 \$04 ADD AX,
 imm16 \$05 ADD r/m8,
 imm8 \$80 xx000xxx
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**Deshmukh Addressing
Mode Of 8086(Part**

1)(\u25a1\u25a1\u25a1\u25a1) 1. Timing

**diagram 8085| Opcode
fetch Assembly**

**Language- Instruction
Set of Intel 8086**

Microprocessor

8086 Instruction

Encoding-8 Addressing

Mode 00! Specifies R/M

Table 1 (with NO

displacement) 000

[BX+SI] 010 [BP+SP] 100

[SI] 110 Drc't Add 001

[BX+DI] 011 [BP+DI] 101

[DI] 111 [BX]! Note that

the 110 case (direct

addressing) requires that the instruction be followed by two address bytes There are then two possibilities: 1 Opcode Addressing Mode
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