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4.26: Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable. Q. 4.23: Draw the logic diagram of 2-to-4-line decoder using (a) NOR gates only (b) NAND gates only **Design of 4 × 4**

RAM || Construction of a 4 × 4 RAM || RAM in computer architecture | 4*4 RAM design Q. 4.3: For the circuit shown in Fig. 4.33 (Section 4.11),(a) Write the Boolean functions Q. 1.1:

List the octal and hexadecimal numbers from 16 to 32. Using A and B for the last two digits Q. 4.8:Design a code converter that converts a decimal digit from the 8, 4, -2, -1 code to BCD Q.

3.29: Implement the following four Boolean expressions with three half adders: $D=A \oplus B \oplus C$ Q. 4.4: Design a combinational circuit with three inputs and one output.(a) The output is 1 when Q. 6.7: Draw the

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sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z

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constructed with four NAND gates and an inverter. Consider the Digital Logic Design - Unit 04 - Combinational Logic - Part 03 - Design Procedure **Q. 3.6: Simplify the following Boolean expressions,**

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